WE CLAIM:

1. A method of testing an apparatus for processing data having a memory operable to store data and a data processing circuit coupled to said memory via a memory access port having a plurality of memory access signal connections, said method comprising the steps of:

testing a subset of said plurality of memory access signal connections using respective associated diagnostic serial scan chain cells each operable to perform at least one of:

(i) applying a diagnostic signal value to a respective memory access signal connection of said subset; and

(ii) capturing a diagnostic signal value from said respective memory access signal connection of said subset; and

testing a remainder of said plurality of memory access signal connections by at least one of:

(iii) outputting a diagnostic signal generated by said data processing circuit to said memory from said data processing circuit via a respective memory access signal connection of said remainder; and

(iv) capturing with said data processing circuit a diagnostic signal input to said data processing circuit from said memory via a respective memory access signal connection of said remainder.

2. A method as claimed in claim 1, wherein said subset includes memory access signal connections which are optionally present within said memory access port in dependence upon a memory size of said memory.

3. A method as claimed in claim 1, wherein said subset includes memory address signal connections from which a diagnostic signal is captured.

4. A method as claimed in claim 1, wherein said data processing circuit includes at least one serial scan chain cell operable to control said data processing circuit to

generate respective diagnostic signals output by said data processing circuit to said memory.

5. A method as claimed in claim 1, wherein said data processing circuit includes at least one serial scan chain cell operable to control said data processing circuit to capture respective diagnostic signals input to said data processing circuit from said memory.

6. A method as claimed in claim 1, wherein said data processing circuit is a processor core.

7. A method as claimed in claim 1, wherein said memory is a tightly coupled memory.

8. A method as claimed in claim 1, wherein said memory has an operational memory size larger that a smallest optional memory size and one or more memory size signals serve to indicate a memory size of said memory, said memory size signals being changed during testing to indicate a test memory size for use when testing said remainder of said plurality of memory access signal connection, said test memory size being smaller than said operational memory size of said memory used during non-test operation.

9. A method as claimed in claim 8, wherein said test memory size is a smallest non-zero memory size which is supported.

10. A method as claimed in claim 8, wherein said memory size signals are changed during testing using signals from one or more serial scan chain cells.

11. Apparatus for processing data, said apparatus comprising:

a memory operable to store data; and

a data processing circuit coupled to said memory via a memory access port having a plurality of memory access signal connections; wherein

a subset of said plurality of memory access signal connections have respective associated diagnostic serial scan chain cells operable to perform at least one of:

applying a diagnostic signal value to a respective memory access signal connection; and

capturing a diagnostic signal value from said respective memory access signal connection; and

a remainder of said plurality of memory access signal connections do not have respective associated diagnostic serial scan chain cells.

12. Apparatus as claimed in claim 11, wherein said subset includes memory access signal connections which are optionally present within said memory access port in dependence upon a memory size of said memory.

13. Apparatus as claimed in claim 11, wherein said subset includes memory address signal connections from which a diagnostic signal is captured.

14. Apparatus as claimed in claim 11, wherein said data processing circuit includes at least one serial scan chain cell operable to control said data processing circuit to generate respective diagnostic signals output by said data processing circuit to said memory.

15. Apparatus as claimed in claim 11, wherein said data processing circuit includes at least one serial scan chain cell operable to control said data processing circuit to capture respective diagnostic signals input to said data processing circuit from said memory.

16. Apparatus as claimed in claim 11, wherein said data processing circuit is a processor core.

17. Apparatus as claimed in claim 11, wherein said memory is a tightly coupled memory.

18. Apparatus as claimed in claim 11, wherein said memory has an operational memory size larger that a smallest optional memory size and one or more memory size signals serve to indicate a memory size of said memory, said memory size signals being changed during testing to indicate a test memory size for use when testing said remainder of said plurality of memory access signal connection, said test memory size being smaller than said operational memory size of said memory used during non-test operation.

19. A method as claimed in claim 18, wherein said test memory size is a smallest non-zero memory size which is supported.

20. A method as claimed in claim 18, wherein said memory size signals are changed during testing using signals from one or more serial scan chain cells.